CLAIMS

1. (Currently Amended) A method for determining unmatched design elements in a circuit comprising the steps of:

determining instances of a first type and a second type of the design elements that are connected to a specific node in the circuit;

storing a gate signal name for each determined said instance of the first type of design element in a first list;

storing the gate signal name for each determined said instance of the second type of design element in a second list;

~~storing~~ determining a cumulative design element characteristic value ~~of~~ by summing a design element characteristic for each determined said instance of the first and the second types of the design elements;

storing the cumulative design element characteristic value in association with the gate signal name;

performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

determining a cumulative value for said design element characteristic, by summing the design element characteristic value corresponding to each said first type of design element gate signal name that matches one of said orphan gate signal names, to produce a total design element characteristic value.

2. (Currently Amended) The method of claim 1, wherein said cumulative design element characteristic value for each determined said instance of the first and the second types of the design elements is stored in a hash table.

3. (Original) The method of claim 1, wherein the first and the second types of the design elements are selected from a family of design elements consisting of transistors, wires, capacitors, resistors, and power sources.

4. (Original) A method for determining unmatched P-FETs and N-FETs in a circuit comprising the steps of:

determining instances of said P-FETs and said N-FETs that are connected to a specific node in the circuit;

storing a gate signal name for each determined said instance of one of said P-FETs in a first list;

storing the gate signal name for each determined said instance of one of said N-FETs in a second list;

storing a cumulative value representing a source current for each determined said instance of said P-FETs and said N-FETs;

performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

determining a cumulative value for said source current, by summing the source current value corresponding to each said P-FET gate signal name that matches one of said orphan gate signal names, to produce a total source current value.

5. (Original) The method of claim 4, wherein said cumulative value representing a source current is stored in a hash table, with a key of the gate signal name and a value of the source current for the determined said instance.

6. (Original) The method of claim 4, wherein said specific node corresponds to a first terminal of said N-FET, and wherein said processor iteratively determines instances of other said N-FETs that are channel-connected to said specific node, until a ground connection is encountered.

7. (Original) The method of claim 6, wherein said first terminal is a source terminal and said second terminal is a drain terminal.

8. (Original) The method of claim 6, wherein said first terminal is a drain terminal and said second terminal is a source terminal.

9. (Original) A system for determining unmatched design elements in a circuit, comprising:

means for determining instances of said P-FETs and said N-FETs that are connected to a specific node in the circuit;

means for storing a gate signal name for each determined said instance of one of said P-FETs in a first list;

means for storing the gate signal name for each determined said instance of one of said N-FETs in a second list;

means for storing a cumulative value representing a source current for each determined said instance of said P-FETs and said N-FETs;

means for performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

means for determining a cumulative value for said source current, by summing the source current value corresponding to each said P-FET gate signal name that matches one of said orphan gate signal names, to produce a total source current value.

10. (Original) A system for determining unmatched design elements in a circuit design, comprising:

a processor for determining instances of P-FETs and N-FETs that are connected to a specific node in the circuit design;

a first list, located in memory coupled to said processor, for storing a gate signal name for each determined said instance of one of said P-FETs;

a second list, located in said memory coupled to said processor, for storing the gate signal name for each determined said instance of one of said N-FETs in a second list;

a storage mechanism for storing a cumulative value representing a source current for each determined said instance of said P-FETs and said N-FETs;

wherein said processor performs a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

wherein said processor determines a cumulative value for said source current, by summing the source current value corresponding to each said P-FET gate signal name that matches one of said orphan gate signal names, to produce a total source current value.

11. (Original) The system of claim 10, wherein said storage mechanism is a hash table, with a key of the gate signal name and a value of the source current for the determined said instance.

12. (Original) The system of claim 10, wherein said specific node corresponds to a first terminal of said N-FET, and wherein said processor iteratively determines instances of other said N-FETs that are channel-connected to said specific node, until a ground connection is encountered.

13. (Original) The system of claim 12, wherein said first terminal is a source terminal and said second terminal is a drain terminal.

14. (Original) The system of claim 12, wherein said first terminal is a drain terminal and said second terminal is a source terminal.

15. (Original) A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining unmatched P-FETs and N-FETs in a circuit comprising:

determining instances of said P-FETs and said N-FETs that are connected to a specific node in the circuit;

storing a gate signal name for each determined said instance of one of said P-FETs in a first list;

storing the gate signal name for each determined said instance of one of said N-FETs in a second list;

storing a cumulative value representing a source current for each determined said instance of said P-FETs and said N-FETs;

performing a set difference operation on the first list and the second list to determine orphan gate signal names that appear in either one of the lists but not in both; and

determining a cumulative value for said source current, by summing the source current value corresponding to each said P-FET gate signal name that matches one of said orphan gate signal names, to produce a total source current value.